Applicant acknowledges and thanks the Examiner for indicating that claims 7-9 are allowable over the prior art and that claims 3-6 would be allowable over the prior art if amended to be in independent form. However, Applicant respectfully submits that all of the presently pending claims recite allowable subject matter and therefore, placing claims 3-6 into independent form is not necessary.

Claims 1 and 2 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Choudhury (U.S. Patent No. 6,229,367). The Office Action asserted that Choudhury discloses all the elements of the claimed invention, except for disclosing an internal circuit coupled to the reset signal. Applicant respectfully submits that claims 1 and 2 recite subject matter that is neither disclosed nor suggested in Choudhury.

Claim 1 recites a semiconductor integrated circuit including a power-on resetting circuit for activating a reset signal in response to an initial supply of a power supply to initialize an internal circuit. The power-on resetting circuit also inactivates the reset signal to a predetermined period after the initial supply to terminate an initialization of the internal circuit. A timing changing circuit is provided for adjusting the predetermined period.

The Office Action took the position that Choudhury discloses the claimed invention. However, it is respectfully submitted that the prior art fails to disclose or suggest such structure and, therefore, fails to provide the advantages that are provided by the present invention. For example, the present invention adjusts the time that the reset signal is inactivated by using the timing changing circuit.

As a result of this claimed configuration, the present invention prevents the reset signal from inactivating before the initialization of the internal circuit terminates and

allows reliable initialization of the internal circuit. Additionally, the present invention enables adjustment of the time that the reset signal is inactivated without directly measuring the timing of the reset signal by utilizing the voltage generator transistor.

Choudhury discloses a time delay system. A selectable asynchronous time delayed signal is generated from an incoming signal using a pulse having a minimum pulse width and a stop-start oscillator. By stopping and re-starting the oscillator for a short duration, in response to a short pulse having a known phase with respect to the incoming signal, the oscillator period does not change with the repetition rate of the incoming signal.

However, contrary to the present invention, Choudhury only appears to disclose a variable delay circuit. There is no disclosure or suggestion of a semiconductor integrated circuit having a power-on resetting circuit, which activates a reset signal in response to an initial supply of a power supply to initialize an internal circuit, and inactivates the reset signal to a predetermined period after the initial supply to terminate an initialization of the internal circuit, as recited in claim 1. As a matter of fact, Choudhury does not disclose any configurations concerning power-on reset circuits, or any operations with respect to a power-on reset circuit.

Therefore, Choudhury cannot have the same effect as the present invention, which is to solve the problem of the reset signal inactivating before the initializing of the internal circuit is terminated, which is a benefit of the claimed configuration. This is done by controlling the inactivation timing (the pulse width) of the reset signal output by the power-on reset signal.

The Office Action took the position that although Choudhury does not disclose an internal circuit, it would have been obvious to one of ordinary skill in the art to utilize the OUT output signal in additional applications. However, the Office Action provided no reference, nor did the Office Action cite any authority in support of this position. Therefore, because Choudhury fails to disclose or suggest this limitation, the Applicant respectfully requests that the rejection be withdrawn.

Furthermore, as claim 2 depends from independent claim 1, Applicant submits that claim 2 also recites subject matter that is neither disclosed nor suggested by the prior art, for at least the reasons set forth above.

Therefore, it is respectfully submitted that the Applicant's invention, as set forth in claims 1 and 2, is not obvious in view of Choudhury within the meaning of 35 U.S.C. § 103.

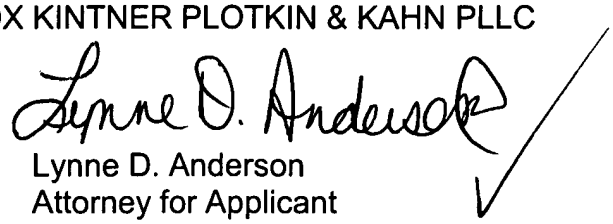
In view of the foregoing, reconsideration of the application, withdrawal of the outstanding rejections, allowance of claims 1, 2 and 10-13 (claims 7-9 already being allowed and claims 3-6 being indicated as reciting allowable subject matter), and the prompt issuance of a Notice of Allowability are respectfully solicited.

Should the Examiner believe anything further is desirable in order to place this application in better condition for allowance, the Examiner is requested to contact the undersigned at the telephone listed below.

In the event this paper is not considered to be timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an

extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 108397-00042**.

Respectfully submitted,
ARENT FOX KINTNER PLOTKIN & KAHN PLLC



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Enclosure: Marked-up Version of Claims

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Marked-Up Version of Claims

1. (Amended) A semiconductor integrated circuit comprising:

a power-on resetting circuit for activating a reset signal in response to an initial supply of a power supply to initialize an internal circuit, and for inactivating the reset signal [for] to a predetermined period after the initial supply to terminate an initialization of the internal circuit; and

a timing changing circuit for adjusting the predetermined period.

7. (Amended) A semiconductor integrated circuit comprising:

a power-on resetting circuit [having a transistor, said power on resetting circuit] configured to inactivate a reset signal which initializes an internal circuit [after activating the reset signal for a predetermined period,] in response to a power supply being switched on, said inactivating performed in a predetermined period after activating the reset signal, and length of the predetermined period being controlled by [utilizing a threshold voltage of the transistor, and to change the time that the reset signal is inactivated in accordance to] a first adjusting signal;

a voltage generator [having a transistor, said voltage generator] configured to receive an external power supply voltage for generating an internal supply voltage [in accordance with an external supply voltage by utilizing a threshold voltage of the transistor, and able to vary], the level of the internal supply voltage [in accordance to] being controlled by a second adjusting signal; [and]

[a timing changing circuit having, said timing changing circuit comprising:]

a programming circuit configured to [store logic values of] output said first adjusting signal and said second adjusting signal; and

a [testing] signal selection circuit configured to [output a test] receive an external signal[, which is supplied from the exterior during a testing mode, as], and to receive said second adjusting signal [and for outputting the logic values stored in] from said programming circuit, to output the external signal to [said power on resetting circuit and] said voltage generator[, respectively,] as [said first adjusting signal and] said second adjusting signal [during a normal operation mode] in response to a test mode signal.

8. (Amended) The semiconductor integrated circuit according to claim 7, wherein said [testing] signal selection circuit includes a mask circuit for masking an output from said programming circuit and for outputting [a testing] said external signal as said second adjusting signal, in response to [a] said test [activating] mode signal which is activated during [said] a testing mode.

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